IN THE CLAIMS

1. (Currently amended) A computer system with a processing unit and a memory, the processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines, each memory line being fetched as a whole and being capable of holding more than one instruction, at least one instruction comprising information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line, the processing unit being arranged to respond to the information by controlling said part as signaled by the information.

2. (Original) A computer system according to claim 1, wherein the information signals explicitly whether or not the subsequent memory line has to be prefetched during processing of the instruction, the processing unit being arranged to start prefetching of the subsequent memory line in response to the information.

3. (Original) A computer system according to claim 2, wherein the information contains a prefetch bit whose value signals explicitly whether or not the subsequent memory line has to be prefetched.

4. (Currently amended) A computer system according to claim 1, wherein the information signals explicitly whether or not an instruction pointer should be updated ~~form~~ from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line is skipped over, the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information.

5. (Original) A computer system according to claim 1, wherein the information signals explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the

processing unit being arranged to stall in response to the information when the instruction is reached from the branching instruction.

6. (Original) A computer system according to claim 1, the processing unit being a VLIW processing unit containing two or more issue slots for issuing operations from the instruction in parallel to the functional units, the instructions being VLIW instructions, capable of containing two or more operations, the instruction comprising a field distinct from the operations to specify said information.

7. (Original) A computer system according to claim 6, the field comprising, in addition to said information, a decompression code that specifies for which issue slots the instruction contains operations.

8. (Currently amended) A method of processing instructions in a computer system with a processing unit and a memory, the processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines capable of holding more than one instruction, at least one instruction comprising information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line, the method comprising fetching each memory line as a whole, processing an instruction from a current memory line, reading the information from the instruction during processing and controlling said part as signaled by the information.

9. (Original) A method according to claim 8, wherein said controlling comprises at least one of causing a subsequent memory line to be prefetched or a program counter to skip to a start of the subsequent memory line or processing to be stalled when the instruction is reached as a branch target.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

IN THE TITLE

Please amend the title to read –VARIABLE LENGTH VLIW INSTRUCTION WITH INSTRUCTION FETCH CONTROL BITS FOR PREFETCHING, STALLING, OR REALIGNING IN ORDER TO HANDLE PADDING BITS AND INSTRUCTIONS THAT CROSS MEMORY LINE BOUNDARIES--